IN THE TITLE

Please replace the title with "TRANSACTION-BASED POWER MANAGEMENT IN A COMPUTER SYSTEM."

IN THE SPECIFICATION

Please replace paragraph [0030] with the following:

--In one embodiment, the power management circuitry 330 communicates with the memory controller 310 and/or the input/output controller 320 via the sideband signals ~~322 and 324~~ 332 and 334. The sideband signals 332 and 334 indicate whether there is any bus mastering activity from a peripheral device, such as an advance graphic port (AGP). The sideband signals 332 and 334 are typically denoted as XX_BUSY. For example, the sideband signal corresponding to the AGP is denoted as AGP_BUSY. One should appreciate that the sideband signals may include one or more shared signals.--

Please replace paragraph [0005] with the following:

--As to the peripheral device, it may be coupled to the CPU through a root complex device via a serial interconnect, such as a PCI ~~Express~~ EXPRESS interconnect. A root complex device includes a host bridge and one or more root ports. Examples of a root complex device include a memory controller or IO controller functional device. An interconnect is an infrastructure that couples one device to another. PCI ~~Express~~ EXPRESS is a high speed, point-to-point serial interconnect standard. For example, the first generation of PCI ~~Express~~ EXPRESS interconnect supports 2.5 Gb/sec per lane data transmission. In one exemplary system, a graphic device is coupled to a chipset of the system (e.g., a memory controller hub) through a 16-lane PCI Express interconnect.--

Please replace paragraph [0006] with the following:

--Furthermore, PCI ~~Express~~ EXPRESS allows flow control by supporting an accounting scheme with credits to keep track of the traffic over a PCI ~~Express~~ EXPRESS interconnect. The credits indicate the available buffering in a device for various types of transactions over an interconnect. For example, a memory controller can report to the software of the capability of a root complex device to transmit data by writing the information in a number of registers. According to PCI ~~Express~~ EXPRESS protocol, there are a number of prescribed credits for various transactions, such as, read request, write request, completion, etc. For example, when a graphic device issues transactions (e.g., read requests) towards the root complex device and these transactions are pending, a credit is consumed to reflect the amount of buffering taken up in the memory controller by the pending transactions. When these transactions are handled or retired by the memory controller, the credit is released or freed up. The number of pending transactions, as reflected by the credits consumed, indicates the likelihood of a bus mastering event that may prohibit entry into the C3 or C4 state.--

Please replace paragraph [0017] with the following:

--A method and an apparatus for power management in a computer system are disclosed. In one embodiment, the method includes monitoring transactions over an interconnect coupling a chipset device and a peripheral device in the computer system, the transactions being transmitted between the peripheral device and the chipset device following a flow control protocol that allows the chipset device to keep track of the transactions. The embodiment further includes causing a processor in the computer system to exit from a power state if a number of coherent transactions pending in a buffer of the chipset device exceed a predetermined threshold. In a specific embodiment, the

flow control protocol is PCI ~~Express~~ EXPRESS. Other features will be apparent from the accompanying figures and the detailed description that follows.--

Please replace paragraph [0029] with the following:

--Figures 3A – 3C illustrate various embodiments of chipset partitions in a computer system. Figure 3A shows a memory controller 310, an input/output controller 320, and power management circuitry 330. The power management circuitry 330 is outside of both the memory controller 310 and the input/output controller 320. The memory controller 310 is coupled to the input/output controller 320 via a link 315. The link 315 may include a digital media interface (DMI) link. The memory controller 310 is further coupled to one or more peripheral devices (not shown) via one or more buses or interconnects (not shown) that adopt a protocol with a credit-based flow control accounting scheme, such as, for example, PCI ~~Express~~ EXPRESS.--

Please replace paragraph [0032] with the following:

-- Figure 3B shows an alternate embodiment of chipset partition in a computer system. The chipset in Figure 3B includes a memory controller 340 and an input/output controller 350 coupling to each other via a link 345, which may include a DMI link. However, one should appreciate that some embodiments of the chipset include additional devices not shown. The memory controller 340 is further coupled to a peripheral device (not shown) via an interconnect (not shown) adopting a credit-based flow control accounting scheme, such as, for example, PCI ~~Express~~ EXPRESS. The peripheral device may include an external graphic core, an Ethernet controller, etc. The input/output controller 350 includes power management circuitry 352 to monitor data traffic over the

interconnect. Since the power management circuitry 352 is internal to the input/output controller 350, the memory controller 340 has to communicate to the input/output controller 350 on whether the peripheral device has any on-going traffic over the interconnect. In one embodiment, the memory controller 340 sets one or more bits in a message packet 347 sent via the link 345 to the input/output controller 350. The message packet 347 may be a DMI packet. Setting the bit(s) in the message packet 347 is also referred to as in-band virtualization of the bus mastering indicator signal, as opposed to the sideband signals (e.g., sideband signals 332 and 334 in Figure 3A), because the signal is abstracted to eliminate the pin and connector infrastructure on both of the controllers 340 and 350. Furthermore, the power management circuitry 352 may also monitor the bus mastering activity from other peripheral devices (not shown) coupled to the input/output controller 350 via other interconnects (not shown).--

Please replace paragraph [0035] with the following:

-- Figure 4 shows an exemplary embodiment of a computer system 400. The computer system 400 includes a central processing unit (CPU) 410, a memory controller (MCH) 420, a number of dual in-line memory modules (DIMMs) 425, a number of memory devices 427, a PCI ~~Express~~ EXPRESS graphic port 430, an input/output controller (ICH) 440, a number of Universal Serial Bus (USB) ports 445, an audio coder-decoder (AUDIO CODEC) 460, a Super Input/Output (Super I/O) 450, and a firmware hub (FWH) 470.--

Please replace paragraph [0036] with the following:

-- In one embodiment, the CPU 410, the PCI ~~Express~~ EXPRESS graphic port 430, the DIMMs 425, and the ICH 440 are coupled to the MCH 420. The link 435 between the MCH 420 and the ICH 440 may include a DMI link. The MCH 420 routes data to and from the memory devices 427 via the DIMMs 425. The memory devices 427 may include various types of memories, such as, for example, dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), double data rate (DDR) SDRAM, or flash memory. In one embodiment, each of the DIMMs 425 is mounted on the same motherboard (not shown) via a DIMM connector (not shown) in order to couple to the MCH 420. In one embodiment, the USB ports 445, the AUDIO CODEC 460, and the Super I/O 450 are coupled to the ICH 440. The Super I/O 450 may be further coupled to a firmware hub 470, a floppy disk drive 451, data input devices 453, such as, a keyboard, a mouse, etc., a number of serial ports 455, and a number of parallel ports 457.--

Please replace paragraph [0037] with the following:

--In one embodiment, the ICH 440 includes power management circuitry 442 to monitor data traffic over various interconnects coupling the ICH 440 and the MCH 420 to the peripheral devices, such as, for example, the PCI ~~Express~~ EXPRESS graphic port 430. The power management circuitry 442 may generate a bus mastering indicator to be sent as a virtualized signal within a message packet 437 from the MCH 420 to the ICH 440 via the link 435. Alternatively, the MCH 420 and the ICH 440 may be integrated into a single controller with power management circuitry such that the bus mastering indicator may be internally registered through logic.--